Coplanar Waveguides on Silicon Substrate with Thick Oxidized Porous Silicon (OPS) Layer

Choong-Mo Nam and Young-Se Kwon

***Abstract*— The problem of high dielectric loss of waveguide on silicon in the microwave region can be solved by utilizing a thick silicon dioxide layer that is formed by silicon substrate anodization and oxidation processes. Coplanar waveguides (CPW's) are fabricated on silicon substrate with a 20-μm-thick oxidized porous silicon (OPS) layer and demonstrate very high performance of 0.1-dB/mm attenuation at 4 GHz. Thus, the OPS process is promising for gigaherz applications of silicon substrates.**

***Index Terms*— Coplanar waveguide (CPW), oxidized porous silicon (OPS), silicon substrate.**

I. Introduction

In the microwave region, several types of transmission line such as microstrip line, coplanar waveguide (CPW), and slot line have been utilized [1]–[6]. The use of uniplanar structure, such as CPW, eliminates the need to perform relatively high risk backside thinning, via etch, and plating step. It is especially well suited for use with field-effect transistors (FET's).

Materials such as gallium arsenide, alumina, diamond, and quartz have been the substrates of choice for microwave application because of their low loss. Although silicon has a very mature technology, low cost, and high thermal conductivity, it has not been used as a microwave substrate because of its extremely high dielectric loss.

Fig. 1 shows some microwave transmission line structures on silicon substrate. The high-resistivity silicon substrate, shown in Fig. 1(a), is widely used for the microwave region because of its low dielectric loss [1]–[3]. But it is not good for integration of silicon active devices such as MOSFET and BiCMOS. To overcome the problem of high dielectric loss of the low-resistivity silicon substrate, a thick SiO_2 layer fabricated by chemical vapor deposition (CVD) method [4], shown in Fig. 1(b), and the technology of spin-coated thick polyimide layer [5], shown in Fig. 1(c), are utilized for microwave applications. In the case of a thick SiO_2 layer fabricated by CVD method, a long process time of SiO_2 deposition and a high process cost are required. Spin-coated thick polyimide has the advantage of simple process and low cost, but it has the disadvantages, such as water uptake and its lifetime is limited. At this point, the oxidized porous silicon (OPS) layer offers many advantages as a microwave material, including: overcoming high dielectric loss of low-resistivity silicon substrate in the microwave frequency range; low fabrication cost and time for the thick SiO_2 layer compare to the CVD method; and negligible water uptake problem in nonhermetic packages.

The problem of high dielectric loss of silicon in microwave region can be solved by utilizing thick silicon dioxide layer which is formed by anodization and oxidation process of silicon substrate. First, the porous silicon layer (PSL) is obtained by anodization process. PSL is oxidized at high temperature with a short oxidation time [7]–[11]. Because the phenomenon of oxidation of porous silicon is due to the reaction of sidewall of trenches, thick oxide layers can be formed very rapidly. These thick oxide layers have been used for the fabrication of integrated circuit [7], [8], optical waveguide [9], microwave package [10], and high-performance microwave planar inductor [11].

In this letter, we fabricated a thick OPS layer on silicon substrate for coplanar waveguide (CPW) with low insertion.

II. Experimental

The OPS layer was obtained by anodization and oxidation process of silicon substrate. PSL was prepared on (100) boron-doped silicon substrate of 8–10 Ω-cm resistivity by an anodization process. The fabrication process of PSL was reported previously [10] and anodic current density was 10 mA/cm^2. The growth rate of PSL is about 0.46 μm/min at the anodic current density of 10 mA/cm^2. The thickness of OPS layer is dependent on PSL thickness, which is determined by anodization conditions such as anodic reaction time and anodic current density. The PSL is preoxidized at 350°C under atmospheric pressure dry oxygen for 30 min. The preoxidized PSL is oxidized for 3 min in wet oxygen at a temperature of 1060°C.

We fabricated CPW on OPS layer with 20-μm-thick SiO_2 as shown in Fig. 2. The CPW lines consist of two consecutive layers of evaporated Ti/Au followed by 2.5-μm Au plating. The center conductor width (W) is 100 μm. But, the gap width (S) varies from 20 to 40 μm. The length of transmission lines is 2 mm. To obtain 50-Ω impedance for CPW on OPS substrate, the W and S values are extracted from the Bedair's equation [12]. In Bedair's equation, the value of ε_r is 3.9.

III. Results and Discussion

For three different CPW gap widths, the insertion losses were measured as a function of frequency and are shown in Fig. 3. Note that the insertion loss of 2-nm-long CPW's is less

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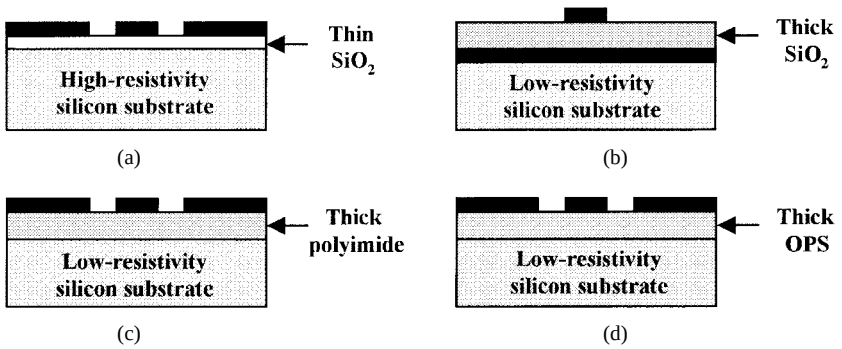

Fig. 1. Structures of microwave transmission lines on silicon substrate. (a) CPW on high-resistivity silicon (HRS) substrate used for low dielectric loss in the microwave frequency range. (b) Microstrip line on thick SiO2 layer fabricated by CVD method. (c) CPW on spin-coated thick polyimide layer. (d) CPW on thick OPS fabricated by anodization and short time oxidation process of silicon substrate.

TABLE I
COMPARISON OF DIFFERENT IMPLEMENTATIONS OF TRANSMISSION LINES ON SILICON SUBSTRATE

Ref.	Transmission line type	Attenuation (dB/mm @4GHz)	Dielectric material(thickness)	Metal for signal line(thickness)	Substrate (resistivity)
[1]	CPW	0.17	SiO_2 (0.9μm)	Al (1μm)	n-type Si (ρ=4kΩ-cm)
[4]	Microstrip	0.12	SiO_2 (9 μm)	Au (3.3 μm)	n-type Si (ρ=0.08Ω-cm)
[5]	CPW	0.19	polyimide (10 μm)	Al (4 μm)	p-type Si (ρ=20Ω-cm)
This work	CPW	0.10	OPS (20 μm)	Au (2.5 μm)	p-type Si (ρ=8Ω-cm)

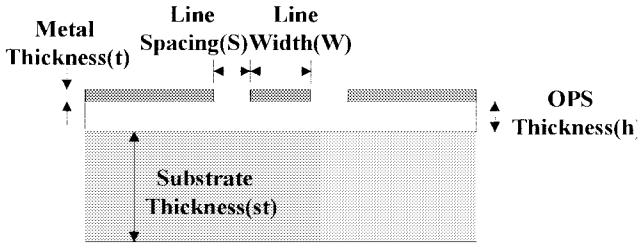

Fig. 2. CPW on thick OPS layer. The microwave passive elements such as high-performance planar inductor, thin film resistor, and MIM capacitor can be fabricated on a thick OPS layer in the microwave frequency range ($W = 100\ \mu\text{m}; S = 20, 30, 40\ \mu\text{m}; t = 2.5\ \mu\text{m}; h = 20\ \mu\text{m}; st = 600\ \mu\text{m}$).

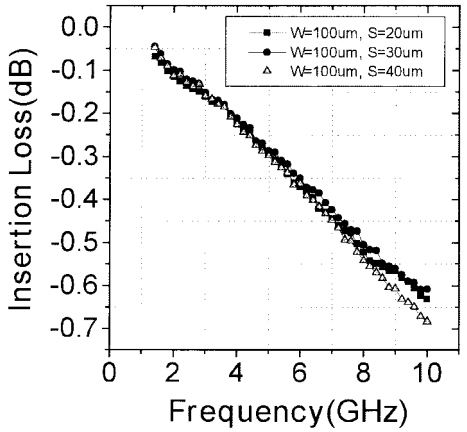

Fig. 3. Insertion loss of CPW on a thick OPS layer as a function of frequency. The insertion loss of CPW ($W = 100\ \mu\text{m}; S = 30\ \mu\text{m}$) of 2-mm length is less than 0.21 dB at 4 GHz.

than 0.21 dB at 4 GHz. Their return losses were measured as a function of frequency and are shown in Fig. 4. Note that

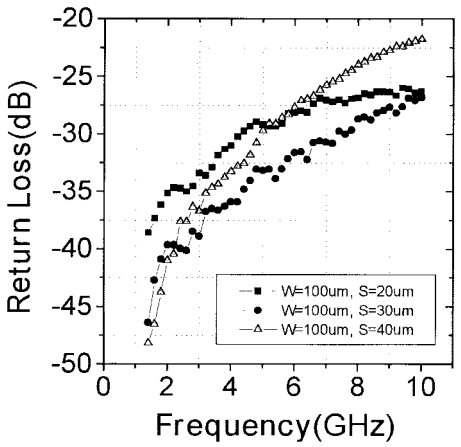

Fig. 4. Return loss of CPW on a thick OPS layer as a function of frequency. The return loss of 2-mm-long CPW's is less than −22 dB at all measured frequency ranges.

the return loss of 2-nm-long CPW's is less than −22 dB at all measured frequency ranges, and very good matching is obtained in case of 30-100-30 (S-W-S) μm. These results agree well with the simulation result of Bedair's equation.

Comparison of different transmission lines on silicon substrate is shown in Table I. In the case of thick OPS layer for dielectric material, the lowest attenuation of signal line was obtained.

IV. CONCLUSION

Instead of direct oxidation of bulk silicon, a short-time oxidation process of porous silicon can be utilized to make a thick oxide layer for microwave waveguides. CPW's on thick OPS layer demonstrated very high performance, such

as low insertion loss, and the OPS layer is very promising for gigahertz application of silicon substrate.

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